

EXHIBIT 7

BBAGG

Volume 2

Implementing Broadband Aggregation on Cisco 10000 Series

Version 1.0

Student Guide

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- Turn the television or radio antenna until the interference stops.
- Move the equipment to one side or the other of the television or radio.
- Move the equipment farther away from the television or radio.
- Plug the equipment into an outlet that is on a different circuit from the television or radio. (That is, make certain the equipment and the television or radio are on circuits controlled by different circuit breakers or fuses.)

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Course Overview

Intended Audience

This course is for technical professionals who need to know how to implement broadband aggregation on the Cisco 10000 Series router. The following are considered the primary audience for this course:

- Customer technicians
- Cisco System Engineers (SEs)
- System Integrators (SIs)

Course Level

This course is basic and intermediate training for the topics that it covers.

Prerequisites

Students attending this course should have successfully completed the following training:

- Interconnecting Cisco Network Devices (ICND) or equivalent experience
- Campus ATM (CATM) or equivalent experience
- Basic DSL End To End Architecture – either video on demand or leader-led or equivalent experience

Module 8

Cisco 10000 Series Router Hardware Overview

Overview

Description

In this module you learn about use of the Cisco 10000 Series Router hardware in broadband aggregation implementations. This module includes descriptions and capabilities of the chassis, PRE-2, and line cards used with broadband aggregation, as well as functional block diagrams of the hardware and packet processing.

Objectives

After completing this module, you will be able to do the following:

- Describe how the Cisco 10000 router is used in typical broadband deployments
- Describe the Cisco 10000 router chassis components
- Identify Cisco 10000 router functional components, interconnections, and operation
- Describe PRE-2 architecture and operation, including the route processor, forwarding processor, and PXF
- Trace the flow of a packet through the PRE-2
- Describe the Cisco 10000 router high-availability hardware and functions
- Describe the features and functions of Cisco 10000 router line cards used with broadband aggregation deployments

Cisco 10000 Series Router Architecture Overview

The pages that follow provide an overview of the Cisco 10000 router architecture. The following topics are presented:

- Functional Block Diagram
- Buffer Management
- Router Backplane

Cisco 10000 Series Router Architecture Overview

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- **Functional Block Diagram**
- **Buffer Management**
- **Router Backplane**

Functional Block Diagram

The major functional components that make up the Cisco 10000 router are the PRE, Iron Bus, and line cards.

PRE-2

The PRE is designed for reliability and high availability. It uses an advanced route processor redundancy (RPR) feature for automatic failover. The PRE is composed of two main sections, a route processor and a forwarding processor.

Route Processor

The route processor provides standard Cisco IOS functionality for:

- Chassis management
- System initialization
- Routing protocol updates
- Route processor redundancy (RPR)
- CLI and SNMP functionality

Forwarding Processor

The forwarding processor provides the following IP functions:

- IP forwarding
- Packet buffering
- Layer 3 features
- QoS features

Three main components make up the forwarding processor:

- Parallel eXpress Forwarding (PXF) engine – a 2-dimensional array of 64 CPUs that forward IP packets. Processor-intensive tasks such as policy routing, quality of service (QoS), and statistics collection are segmented and distributed to columns of multiple processors.
- Packet Buffers – buffer packets processed by the PXF engine.
- Cobalt ASIC – provides buffer management and Iron Bus data flow control. It controls the flow of packets from the line cards to the forwarding processor, ensuring that the PXF does not become overloaded. In addition, it manages the queuing and dequeuing of packets to the 256MB packet buffers under the direction of the PXF.

Functional Block Diagram

